

# (SYLLABUS)

1.

(Course Title)		(Instructor)			
(Year)	2022	(Semester)	1	(Course No.)	2150078601
(Class)	01	(Open to)		(Course Classification)	-
(Credit)	3.0		03		100
					Office Hour
(Office)	051301	(Telephone)	02-820-0638	(e-mail)	donghwashin@ssu.ac.kr
	(*) (ABEEK Classification)		(*) (ABEEK Requirement)		
(Course Description)					

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가	( 100 )	
	25	25
RTL	30	30
Verilog	25	25
FPGA	20	20

(Required Texts)		
	( )	* /Digital Design/F. Vahid/Wiley/2011/2nd ed. * / / : , L. / /2016/2

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2.

(Week)	(Keyword)	(Description)		(Texts)
01	,	• • • / /	,	
02	,	• • / ( )	,	
03		• 2 •K-Map 2	,	
04	1	• ; /	,	
05	2	• ; /	,	
06	Testbench,	•Schematic/Verilog HDL •Testbench	,	
07		Full Adder	,	
08		( )	,	
09	,	•1 • SR latch •JK-, D- Flip-Flop	,	
10		•Clocks •	,	
11	Finite State Machines 1	•FSM(Finite State Machine) •FSM	,	
12	Finite State Machines 2	•FSM •	,	
13	Counter	Decimal Counter	,	
14		Multi-function Counter	,	
15		( )	,	

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3. ( )

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	Open-ended problem		
	Teamwork		
	Communication skills		